REMARKS

Present Status of Application

The Examiner is thanked for the thorough examination of the present application. The Office Action, however, tentatively rejected all twelve of the originally-filed claims. In view of the amendments made herein, and the remarks set forth below, Applicants respectfully request that the rejections be reconsidered and withdrawn.

Inconsistencies in the Office Action

Before addressing the specific rejections of the Office Action, Applicants respectfully submit that the Office Action has taken certain inconsistent positions. As one example, the Office Action has rejected claim 6 under both 35 U.S.C. § 112, second paragraph, as well as 35 U.S.C. § 102 as allegedly anticipated by U.S. Patent 6,172,906 (hereafter the '906 patent). In setting forth the rejection under 35 U.S.C. § 112, second paragraph, the Office Action stated that "it is unclear what may be the 'third integrated circuit'." (Office Action, sentence spanning pages 2 and 3). In connection with the rejection under as 35 U.S.C. § 102, the Office Action alleged that elements 669 and 674 of the '906 patent constitutes the claimed "third integrated circuit." Thus, on the one hand, the Office Action states that the claim element of the "third integrated circuit" is unclear, yet on the other hand, the Office Action applies teachings from the '906 patent as allegedly clearly anticipating the "third integrated circuit." If the claim element is so unclear as to not comply with 35 U.S.C. § 112, second paragraph, the undersigned fails to see how the Examiner can sufficiently understand this element to apply prior art as "clearly anticipating" the element.

Discussion of Rejections Under 35 U.S.C. § 112, Second Paragraph

The Office Action rejected all claims 1-12 under 35 U.S.C. § 112, second paragraph for various, stated reasons. Applicants respectfully submit that, in view of the

above amendments and following remarks, that each of these rejections should be withdrawn. In this regard, claims 1, 2, 3, 8, 10, and 12 were rejected for the use of the term "logic," and the Office Action suggested that the term "logic block" or "logic circuit" should be used instead. Applicant has amended the claims to adopt Examiner's suggestion of the term "logic block."

The Office Action rejected independent claims 1, 6, 9, and 11 under 35 U.S.C. § 112, second paragraph alleging that either "essential structural cooperative relationships between" various claimed components is missing, or that "it is unclear what may be the structural relationships between" certain claimed components. (Citing MPEP § 2172.01). Applicants respectfully disagree. As an example, Applicant refers to claim 6, which recites " a host integrated circuit component," "a first integrated circuit component," "a second integrated circuit component," and "a third integrated circuit component." As clearly described in the specification, and with reference to Fig. 2, the host integrated circuit component corresponds to reference numeral 102, the first integrated circuit component corresponds to reference numeral 214 of element 210, whereas the second integrated circuit component corresponds to reference numeral 214 of component 211. Finally, the third integrated circuit component corresponds to either component designated by reference numeral 215.

Claim 6 clearly defines how the first integrated circuit component 214 of component 210 interfaces with a first portion of the system bus, whereas the second integrated circuit component 214 of component 211 interfaces with a second portion of the system bus. The third integrated circuit component 215 communicates with the host 102 via the first and second integrated circuit components, and, as is illustrated in Fig. 2 as well as defined in claim 6, the third integrated circuit component 215 is not directly coupled with the system bus 105. Accordingly, Applicants submit that the subject matter set forth in the claim

clearly complies with all statutory requirements. Likewise, independent claims 1, 9, and 11 recite similar structural specificity as to comply with all statutory requirements of the claims. Should the Examiner find parts of these claims unclear, Applicants respectfully request that the Examiner recite, with specificity, what he believes to be unclear with the claims. Merely stating certain basic elements of the claims with the conclusory statement that "essential structural cooperative relationships between the" components is omitted is insufficient to comply with the administrative requirements imposed upon Examiners for carrying out a thorough examination of the application. Again, should the Examiner set forth, with specificity, features that the Examiner considers to be unclear within the claims, then the undersigned will be happy to address these in an ensuing response.

Relatedly, the Office Action rejected claim 6 stating that it is unclear what may be the "third integrated circuit." In response, Applicants direct the Examiner's attention to Figs. 2-6 and the discussion of the "split bus logic" elements denoted by reference numerals 215, 315, and 415a and 415b of those embodiments. These elements correspond to the "third integrated circuit" element of claim 6.

In view of the foregoing, Applicants respectfully submit that all claims, as amended, fully comply with the requirements of 35 U.S.C. § 112, second paragraph, and Applicants respectfully request that the rejections thereof be reconsidered and withdrawn.

Discussion of Rejections Under 35 U.S.C. § 102

The Office Action rejected claims 1-6 and 8-12 under 35 U.S.C. § 102(b) as allegedly anticipated by the '906 patent. For at least the reasons set forth below, Applicants respectfully disagree and request that the rejections be reconsidered and withdrawn. With regard to claim 1, claim 1 recites:

> 1. An ***integrated circuit component*** comprising:
>
> a logic block capable of being ***configured to interface with a first companion integrated circuit*** and to receive information that is communicated from the first companion integrated circuit, which information ***was communicated to the first companion integrated circuit via a first portion of a system bus***; and
>
> a logic block capable of being ***configured to interface with a second companion integrated circuit*** and to receive information that is communicated from the second companion integrated circuit, which information ***was communicated to the second companion integrated circuit via a second portion of the system bus, wherein the first companion integrated circuit and the second companion integrated circuit are disposed in separate integrated circuit chips.***

(*Emphasis added*). Applicants respectfully submit that claim 1 patently defines over the '906 patent for at least the reasons that the '906 patent fails to disclose the features emphasized above.

Notably, claim 1 is directed to "an integrated circuit component" (i.e., a single component) that includes two separate logic blocks. A first logic block is capable of being configured to interface with a first companion integrated circuit and to receive information that is communicated from the first companion integrated circuit, which information was communicated to the first companion integrated circuit via a first portion of the system bus. Likewise, the second logic block is capable of being configured to interface with a second companion integrated circuit and to receive information that is communicated from the second companion integrated circuit, which information was communicated to the second companion integrated circuit via a second portion of the system bus. Simply stated, these features are not disclosed in the '906 patent.

To assist the Examiner in a better understanding of claim 1, consider the embodiment of Fig. 6 of the present application. The first companion integrated circuit corresponds to reference numeral 210, while the second companion integrated circuit corresponds to reference numeral 211. The first logic block corresponds to split bus logic 415a, while the second logic block

corresponds to split bus logic 415b. As is illustrated in Fig. 6, and more particularly claimed in claim 1, the first logic block (e.g., split bus logic 415a) is capable of being configured to interface with a first companion integrated circuit 210 and to receive information that is communicated from the first companion integrated circuit via a first portion of a system bus 105. Likewise, the second logic block (e.g., split bus logic 415 b) is configured to communicate and receive information that is communicated over a second portion of a system bus and routed through the second companion integrated circuit 211.

Similarly, claim 1 also covers the embodiment of FIG. 2. In this regard, the first companion integrated circuit corresponds to reference numeral 210, while the second companion integrated circuit corresponds to reference numeral 211. The first logic block corresponds to the split logic block 214 of component 210, while the second logic block corresponds to split bus logic 215 of component 211.

The teachings applied by the Office Action from the '906 patent (disclosing two memory chips 670 and 672 of a memory bank 506) are simply inapplicable to the embodiments of the invention as defined by claim 1. For at least this reason, the rejection of claim 1 should be reconsidered and withdrawn. As claims 2-5 depend from claim 1, the substantive rejections of those claims should be withdrawn for at least the same reasons.

With regard to independent claim 6, claim 6 recites:

> 6. A system in which a plurality of companion integrated circuit components collectively implement a logic function embodied in a single, conventional integrated circuit component, comprising:
> a host integrated circuit component communicating with other integrated circuit components via a system bus;
> a first integrated circuit component comprising logic for interfacing with a first portion of system bus;
> a second integrated circuit component comprising logic for interfacing with a second portion of system bus;
> a third integrated circuit component not directly coupled with the system bus and comprising logic for communicating with the host integrated circuit via the first and second integrated circuit components, ***wherein the first***

> ***integrated circuit component, the second integrated circuit component, and the third integrated circuit component are provided in physically integrated circuit chips.***

(*Emphasis added*). Applicants respectfully submit that claim 6 defines over the '906 patent for at least the reasons that the '906 patent fails to teach those features emphasized above.

As amended, claim 6 specifies that the first integrated circuit component and the second integrated circuit component are separate integrated circuit chips. As described in the specification of the present application, one benefit of the present invention is realized through the reduction in pin count on integrated circuit packages by distributing functionality across multiple integrated circuit packages, whereby each package may have certain conductive pins that interface with only a portion of the system bus (thereby reducing the pin count for a given IC chip). An embodiment covered by claim 6 includes a system comprising a host integrated circuit 102, a first integrated circuit component, a second integrated circuit component, and a third integrated circuit component. As previously described herein, claim 6 reads on the embodiment illustrated in Fig. 2, wherein the first integrated circuit component includes split bus logic 214 of component 210, whereas the second integrated circuit component includes split bus logic 214 of integrated circuit component 211. As is illustrated in the diagram of Fig. 2, integrated circuit components 210 and 211 are physically separate integrated circuit chips. The third integrated circuit component comprises split but logic 215 which, as illustrated, is not directly coupled with the system bus 105, but can nevertheless communicate with the host 102 by way of split bus logic 214.

Similarly, claim 6 reads on the embodiment illustrated in Fig. 6, wherein the third integrated circuit component may comprise either split bus logic 215 or split bus logic 415 (e.g., 415a and/or 415b).

Simply stated, the teachings of the '906 patent are not applicable to the embodiments defined by claim 6, as the '906 patent fails to disclose at least the third integrated circuit component. Specifically, claim 6 defines the first, second, and third integrated circuit components as comprising separate integrated circuit chips, and it is clear that the applied element (reference numeral 669 of the '906 patent) does not comprise a physically separate integrated circuit chip from reference numeral 670, which is applied as allegedly comprising the second integrated circuit component. Accordingly, the rejection of independent claim 6, as well as dependent claims 7 and 8, should be withdrawn.

With regard to independent claim 9, claim 9 is directed to an embodiment that reads on, for example, the embodiment illustrated in Fig. 6. Significantly, claim 9 is directed to an integrated circuit 410 that comprises two sets of conductive pins for channeling communications to a host integrated circuit 102 through two intermediate integrated circuits 210 and 211. The teachings of the '906 patent disclose a data bus that has a portion connected to a first flash memory 670 and a second portion of the data bus coupled to a second flash memory 672. Significantly, however, there is no disclosure in the '906 patent of an integrated circuit that is coupled to a host integrated circuit via two intermediate integrated circuits, as is specifically claimed in claim 9. For at least this reason, the application of the '906 as a anticipatory reference to claim 9 is misplaced, and the rejection should be withdrawn. Likewise, the rejection of claim 10, which depends from claim 9 should be withdrawn as well.

Finally, Applicants refer to independent claim 11 which is directed to an integrated circuit (see, e.g., Figs. 2-4) having two independent logic portions, with each logic portion being "alternatively configured to communicate with a host integrated circuit via a portion of the system bus and a companion integrated circuit..." There is

no teaching whatsoever, in the '906 patent of logic portions that are configurable to alternatively communicate either directly with a host component (e.g., split bus logic 214 of Fig. 2) or to be configured to communicate with a companion integrated circuit (e.g., split bus logic 215 of Fig. 2). The Office Action appears to rely on the word "or" in the original claim as requiring "only one condition" in order for the prior art to meet the claim limitations. As amended, the term "or" has been removed from claim 11 and all claim limitations now must be considered. For at least the reasons stated above, claim 11 patently defines over the '906, and the rejection thereof should be withdrawn. For at least the same reason, the rejection of dependent claim 12 should be withdrawn as well.

Double Patenting Rejections

Claims 1-12 were rejected under the judicially created doctrine of obviousness-type double patenting. A terminal disclaimer is submitted herewith to address and overcome this rejection.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fees are believed to be due in connection with this amendment and response. If, however, any fees are deemed to be payable, you are hereby authorized to charge any such fees to Hewlett-Packard Company's deposit account No. 08-2025.

Respectfully submitted,

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